IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	Philip KELLER	Confirmation No.:	2466
Application No.:	09/413,821	Group Art Unit:	2611
Filed:	October 7, 1999	Examiner:	Tesfaldet Bocure

For: AUTOMATIC OUTPUT DRIVE LEVEL CONTROL IN HOME NETWORKING TRANSCEIVER

Commissioner for Patents
Alexandria, VA 22313-1450

REPLY BRIEF

Dear Sir:

This Reply Brief is submitted in response to the Examiner's Answer mailed October 26, 2009.

I. STATUS OF THE CLAIMS

Claims 1 through 16 are pending in this application. Claims 5 through 16 stand allowed. Claims 1 through 4 stand finally rejected in the Office Action dated March 4, 2009. Claims 1 through 4 are on appeal.

II. GROUNDS OF REJECTION TO BE REVIEWED

Claims 1 through 4 were rejected under 35 U.S.C. §103(a) for obviousness based on Cheng et al. (US 6,377,666).

III. ARGUMENT

Appellant maintains and incorporates the positions presented in the Appeal Brief filed August 24, 2009, but presents further refutation of certain assertions presented in the Examiner's Answer.

Independent claim 1 recites, *inter alia*, "comparing a controlled value representing the DC level with a predetermined threshold level, and controlling the output driver until the controlled value is equal to the threshold level." As explained in the principal Brief, Cheng et al. do not compare a controlled value representing the DC level set at the output transmit terminal with a predetermined threshold signal to control the output driver until the controlled value is equal to the threshold level. The Examiner responded, at page 6 of the Answer, by contending that "the logic unit [in Cheng et al.] **should have a comparator** for generating the power level shown in figures 4A and 4B, see upper and low voltage levels. Therefore, the logic **unit should compare** the desired voltage value according to the high and low voltage levels, claimed threshold, in order to generate the signal to control the driver" (emphasis added).

What a reference "should" or "should not" have is irrelevant to a determination of obviousness, the proper test being based on what a person of ordinary skill in the art would have been led to do from the prior art teachings. The indisputable fact that Cheng et al. do not disclose or suggest a comparison of a controlled value with a predetermined threshold value remains. The Examiner's wishful thinking that the reference ought to, or "should," comprise or teach such a comparison does not change this fact.

Figures 4A and 4B of Cheng et al, on which the Examiner relied, depicts a high power mode and a low power mode, respectively, of an output signal from the current amplifier. The

high power mode waveform of Figure 4A depicts an upper value of about 2.20 volts while the low power mode waveform of Figure 4B depicts an upper value of about 1.95 volts. Because these waveforms have upper (and lower) values, the Examiner seems to think that the specific peak-to-peak values can only be achieved with threshold values and a comparator for comparing the threshold values with current values, so as to restrict voltage values to those threshold values. But such a synopsis can only be derived from a figment of the Examiner's fertile imagination because there is no basis for this rationale within the disclosure of Cheng et al. In fact, the waveforms of Figures 4A and 4B may not be derived from any thresholds and/or comparators at all. It may very well be that since control logic 201 controls the operation of the DACs 203 and 205 (col. 4, lines 27-28), the control logic 201 determines the upper and lower voltages of the waveforms and feeds this voltage to DACs 203 and 205 for input to the current amplifier 207 for output, in which case, the upper and lower waveform voltages of Figures 4A and 4B are predetermined and issued by the control logic 201 rather than by continuously comparing a current voltage to a threshold value and clipping the current voltage at that threshold value. In fact, since Cheng et al. disclose the logic control as generating the voltage control negative (Vcn) and the voltage control positive (Vcp) to supply the DACs 203 and 205, along with the selection of the power mode level (col. 4, lines 27-51), it appears more likely than not that the control logic 201, and not a comparator/threshold combination, determines and provides for the upper and lower voltages of the depicted waveforms. In any event, the Examiner's conclusion that the upper and lower power levels are (or "should" be) provided by a comparison against threshold values, is, at best, based on pure speculation. It is up to the Examiner, in the first instance, to provide a factual basis to support a conclusion of obviousness and **deficiencies in the factual basis cannot be supplied by resorting to speculation** or unsupported generalizations. *In re*

Freed, 425 F.2d 785, 165 USPQ 570 (CCPA 1970); *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). Based on the evidence of record, it cannot reasonably be concluded that Cheng et al. suggest or make obvious, within the meaning of 35 U.S.C. §103(a), "comparing a controlled value representing the DC level with a predetermined threshold level, and controlling the output driver until the controlled value is equal to the threshold level."

Accordingly, Appellant submits that the imposed rejection of claims 1 through 4 as being obvious over Cheng et al. under 35 U.S.C. §103(a), is not factually or legally viable and, hence, solicits the Honorable Board to reverse the rejection.

IV. CONCLUSION AND PRAYER FOR RELIEF

The claims require "comparing a controlled value representing the DC level with a predetermined threshold level, and controlling the output driver until the controlled value is equal to the threshold level," but Cheng et al. fail to disclose or suggest these claim features. Appellant, therefore, requests the Honorable Board to reverse the Examiner's rejection of claims 1 through 4 under 35 U.S.C. §103(a).

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 504213 and please credit any excess fees to such deposit account.

Respectfully Submitted,

DITTHAVONG MORI & STEINER, P.C.

December 14, 2009
Date

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